Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-6. (Canceled)

7. (Previously Presented) A monolithic structure effective to implement an emitter switching configuration, comprising at least one bipolar transistor and a MOS transistor having a common conduction terminal; at least one substrate having a first conductivity type whereon a first buried layer having a second conductivity type and a second buried layer having said first conductivity type are formed, said first and second buried layers covered by an epitaxial layer having said first conductivity type, said first buried layer forming, by means of first wells of said second conductivity type a control terminal of said bipolar transistor, and said second buried layer forming said common conduction terminal; and second wells of said first conductivity type, adjacent to said first wells of said second conductivity type and in contact with said first wells and with said second buried layer to define a Zener diode parallel to a junction defined by said first and second buried layers with a node of the Zener diode coupled to the control terminal of the bipolar transistor and a cathode coupled to the common conduction terminal.

8. (Original) The monolithic structure of claim 7 wherein said first and second wells are more heavily doped than the first and second buried layers.

9. (Currently Amended) ~~An emitter switching circuit, comprising a bipolar transistor having a base-to-emitter device coupled to a drain terminal of a MOS transistor and configured to prevent a breakdown condition of a body-drain junction of the MOS transistor, the base-to-emitter device comprising a Zener diode, having~~ The monolithic structure of claim 7, wherein the Zener diode has a lower Zener voltage than a breakdown voltage of a junction

between the ~~base and the emitter~~ control terminal of the bipolar transistor and the common conduction terminal.

10-12. (Canceled)

13. (Original) An integrated emitter switching circuit, comprising:

a substrate of first conductivity type having a first layer formed thereon of a second conductivity type and a second layer formed on said first layer of the first conductivity type, and an epitaxial layer covering the first and second layers, the epitaxial layer having the first conductivity type;

first wells of the second conductivity type formed in the epitaxial layer to contact the first layer and second wells of the first conductivity type formed in the epitaxial layer adjacent to and in contact with the first wells and with the second layer to define in combination with the first wells a Zener diode having an anode terminal connected to a base terminal of a bipolar transistor formed in association with the epitaxial layer and a cathode terminal coupled to an emitter terminal of the bipolar transistor and a drain terminal of a MOS transistor formed in association with the epitaxial layer.

14. (Original) The integrated circuit of claim 13 wherein the first and second wells are doped such that a breakdown voltage of a junction between the first and second wells is lower than a breakdown voltage of a junction formed between the base terminal and the emitter terminal of the bipolar transistor.

15. (Original) The integrated circuit of claim 14, further comprising first and second double diffusing regions of the second conductivity type formed in the epitaxial layer, each double-diffusion region comprising first and second high-concentration double-diffusion regions of the first conductivity type formed therein and corresponding to source regions of the MOS transistor, and further comprising a polysilicon structure formed on the epitaxial layer and in communication with the high-concentration double-diffusion regions of the first and second double-diffusion regions to form a gate terminal of the MOS transistor.

16. (Original) The integrated circuit of claim 15 wherein the first wells also contact the second layer.

17. (Currently Amended) ~~A circuit, comprising:~~The integrated circuit of claim 13, wherein:

~~at least one~~ the bipolar transistor ~~having~~ includes a collector terminal~~,~~ and an emitter terminal~~, and a~~ along with the base terminal;

~~at least one~~ the MOS transistor ~~having~~ has a gate terminal~~,~~ and a ~~first~~ collector terminal~~, and a second terminal, the first~~ along with the drain terminal of the MOS transistor coupled to the emitter terminal of the bipolar transistor at a first node; and

~~a~~ the Zener diode ~~having an anode terminal coupled to the base terminal of the bipolar transistor and a cathode terminal coupled to the first node, the Zener diode~~ configured to have a lower Zener voltage than a breakdown voltage between the base terminal of the bipolar transistor and the first terminal of the MOS transistor.

18. (Canceled)

19. (Previously Presented) The circuit of claim 17, wherein the MOS transistor comprises a vertical double-diffusion type transistor.